Multi-Time Write Antifuse (2^nTP) Bridges the Gap Between OTP and FTP/MTP Non-Volatile Memories

March 2010

By: Walter Novosel, Novocell Semiconductor

Abstract

Since the introduction of one-time programmable (OTP) memories, customers have been forced to weigh the benefits between OTP, few-times programmable (FTP), and multi-time programmable (MTP) non-volatile memories. With the release of Novocell's multi-time programmable anti-fuse technology (2^nTP), customers now have the choice of a NVM memory with OTP security and reliability as well as the multi-time programmable benefit of MTP.

In the programmable non-volatile memory market, a gap exists between multi-time programmable memories and one-time programmable memories. Users are forced to choose between 100-100,000 time write functionality and one time write functionality. To fill this 2-100 time write gap, users make area, security, and cost tradeoffs by either cascading multiple OTP blocks or by using one of the larger FTP/MTP solutions to meet their limited multi-time write functionality requirements. Novocell's new 2^nTP offers unique solution to truly bridge the gap, offering a non-volatile memory with OTP security and reliability as well as multi-time write programmability.

The current NVM market is divided into three categories:

- Multi-Time Programmable (MTP): programmable to ~100,000 writes. These memories use floating gate and charge trapping technologies.
- One-Time Programmable (OTP): programmable to one write. These memories utilize gate oxide breakdown (antifuse technology), hot carrier injection, or poly fuse solutions.
- Few-Time Programmable (FTP): programmable up to ~100 writes. These memories utilize floating gate technology.

The release of 2^nTP creates a new category:

- Multi-Time Programmable Antifuse (2^nTP): programmable to 2, 4, or 8 writes. These memories utilizes gate oxide breakdown (antifuse technology).

1.0 Programmable NVM Solution Comparison

	MTP	OTP	FTP	2^nTP
Cell Structure	Floating Gate	Poly Fuse or Antifuse	Floating Gate	Antifuse
Standard CMOS Compatible	No	Yes	Yes	Yes
Number of Writes	~100,000	1	~100	2,4,8
Life Time	~10 Years	~5-15 Years	~10 Years	30+ Years
Area (Normalized)	3	1	3	1.4

Figure 1: Programmable NVM Solution Comparison

2.0 MTP Memories

Multi-time programmable (MTP) memories offer the most flexibility with an average of ~100,000 write and erase cycles. These memories are expensive and less scalable to the smaller geometry nodes. The greater cost of these memories is due in part to the embedded Flash process that uses at least ten additional mask or post processing steps. The limited scalability to faster nodes is the result of the thick oxides required by floating gate memories. These oxides range in size from as 50 angstroms, but typically 70 angstroms and must be carefully monitored to ensure that the programming charge is maintained over the lifetime of the memory.

Size is also a concern with MTP designs. The cell size in floating gate structures is approximately 3 times larger than OTP designs, forcing the user to allocate significant die area.

Due to the ability to erase data, security concerns exist with MTP memories. The data stored in MTP memories is vulnerable to hackers who can adjust, tamper with, or reverse engineer the memory to read out the existing (stored) data or security codes.
While MTP memories may give users the most flexibility and the greatest number of write/erase cycles (~100,000), there are cost, area, reliability, and security tradeoffs.

3.0 – OTP Memories

One-time programmable (OTP) memories have been available in the industry for many years. The first OTP memories were available in the form of polyfuses or eFuse technology. These memories are programmed by forcing a high current through a poly silicon link in order to changes the resistance to a higher level. Polyfuse technology added a level of security because the stored data could no longer be erased and rewritten. However, this security improvement was limited by the poor reliability of polyfuse technology.

Antifuse technology, first introduced nine years ago, offered an alternative to polyfuse OTP. Antifuse technology utilizes breakdown of the gate oxide as the programming mechanism for OTP memory. Process costs are reduced with antifuse technology because it can be manufactured in standard CMOS processes without additional process steps.

Antifuse technology is inherently more secure than floating gate technology because the oxide breakdown is so small that it is difficult to detect, and once broken down it cannot be altered. Antifuse technology is reliable up to extremely invasive reverse engineering techniques, whereas, floating gate technologies are susceptible up to level I (non-invasive attacks such as glitching, power analysis, or data stream analysis) and level II attacks(semi-invasive attacks including UV attacks, microscopy, fault injection, voltage contrast, or magnetic scans).

OTP memory has a variety of applications although customers can often require more than a single write cycle. Customers often need the security of OTP antifuse technology but also need more than one write cycle. Currently, the solution for this multiple write functionality is that the OTP providers cascade multiple OTP blocks together, providing separate blocks for each write. However, this duplicates much of the programming and sensing circuitry, quadrupling the area for a 4x write. For example, if a customer wants 2x write, the area will double. With a 4x write, the area will quadruple. In addition to these area increases, the cost of implementing two or four blocks can double or quadruple proportionately. This is a significant disadvantage for customers who need to program the memory at wafer for internal testing then reset the part for a customer's own configuration. A gap tradeoff still exists between MTP and OTP benefits and disadvantages.

4.0 FTP Memories

Few-time programmable memories (FTP) have recently been developed in an attempt to bridge the gap between OTP and MTP memories. FTP memories offer users ~100 time writes in a standard CMOS process but typically require post processing steps. FTP memories utilize floating gate architecture and thus are prone to the same security and reliability limitations of floating gate MTP memories.

These limitations include the security concerns of memory tampering and security code extraction, area constraints, and the strict control required to monitor the gate oxide and maintain charges.

5.0 Novocell 2^nTP

Novocell has developed a non-volatile memory (NVM) to bridge the gap between the multi-time write benefits of MTP and the security, cost and area benefits of OTP. Novocell's 2^nTP offers an alternative to the cascaded OTP block solution for multiple time functionality. 2^nTP is a single antifuse memory block which can support up to 8 time writes. 2^nTP utilizes Novocell's patented SmartBit architecture to support multiple antifuse devices within a single bit cell, eliminating the need for additional duplicated circuitry. This gives users a 60% area savings over using multiple OTP blocks. Because 2^nTP is based on the industry and silicon proven NovoBlox OTP, the technology maintains the 100% reliability (zero tail bit failures) and more than 30 years of data retention. Like other antifuse technologies, 2^nTP can be embedded in standard Logic CMOS and does not require additional process or mask steps.

2^nTP applications include any instance when multiple OTP blocks would be used.

Two-times write example:

- Order changes – If a product is calibrated for a specific user and the order is cancelled, 2^nTP memory allows the user to reprogram the part to be used by another customer.

Four-times write example:

- Feature testing – If a product needs to be tested and calibrated at wafer, at package, at distribution, and then finally by the customer.

6.0 Conclusion

2^nTP memory bridges the gap between OTP technologies and MTP technologies by offering the area, security, and reliability advantages of OTP memory and the multi-time write functionality of MTP memory. 2^nTP offers an area efficient and less costly solution for secure multi-time programmable NVM applications.

Since 2^nTP memory utilizes Novocell's SmartBit technology, 2^nTP customers receive the industry leading reliability of Novocell's antifuse OTP technology, which guarantees 100% programming reliability with 30+ years' data retention.

For more information regarding Novocell's 2^nTP multi-time write technology or Novocell's NovoBlox OTP technology, please visit www.novocellsemi.com or email info@novocellsemi.com

Author Bio: Walter Novosel is the Engineering Director at Novocell Semiconductor. He has been in the industry 10 years focusing on NVM and Antifuse memories. Mr. Novosel has helped guide Novocell to be the industry leader in antifuse reliability and performance. He has been instrumental in the development of the 2^nTP technology.