

Importance of Dynamic Programming for Achieving Hard Breakdown in Anti-Fuse Technology

By: Walter Novosel, Novocell Semiconductor

Abstract

As System-on-chip (SOC) developers continue to look for ways to reduce cost and time to market, it is important to consider the different non-volatile memory (NVM) options that add flexibility to their products. Over the last few years, the NVM market has been flooded with new solutions. Now, having customers weigh the benefits of reliability, options, and costs during project development is even more critical. With antifuse vendors targeting a wider range of functionality and products, noting the reliability concerns of reaching hard breakdown (HBD) compared to soft breakdown (SBD) is vital.

Antifuse technology is the opposite of fuse technology. When a fuse is programmed, the conduction path is destroyed, resulting in high resistance. In an antifuse device, the circuit begins in a high resistance state, and maintains a low resistance state when programmed.

The resistance change is achieved by applying a high voltage to the programming gate. Hard breakdown occurs after several stages of programming.

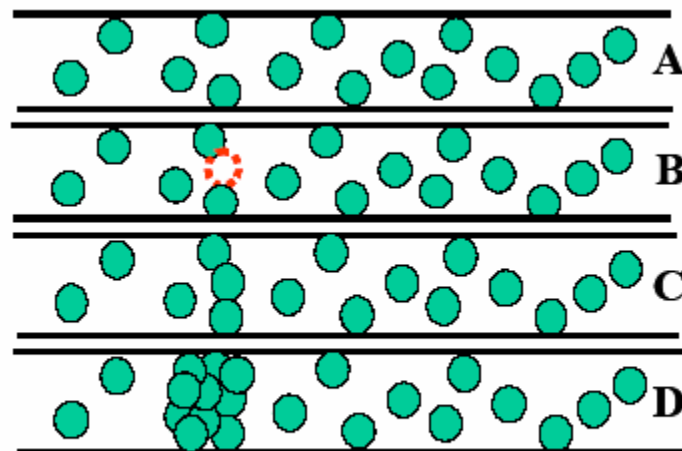


Figure 1 Sequence for breakdown process

- A. Normal gate with no stress. Only natural defects present and depending on proximity, gate leakage can occur.

- B. Stress-Induced Leakage can induce a possible situation where Soft Breakdown can occur. The dotted circle can either remain, leading to Soft Breakdown; or dissipate and revert back to a normal gate.
- C. Soft Breakdown has occurred and a small filament made up of trapped charges has formed. This stage paves the way to Hard Breakdown but is NOT a permanent change.
- D. Hard Breakdown has occurred due to thermal meltdown and a strong irreversible filament has been formed.

Stage 1

Defect Generation or Stress-Induced Leakage Current

The first stage of oxide breakdown is oxide wear or trap charge generation. During initial programming, microscopic defects, or traps, are generated in the SiO₂ layer during electric field stress. These defects lead to increased leakages across the gate. Three mechanisms can lead to this increased leakage current:

- Direct Tunneling – Requires a fairly thin oxide for significant current
- Fowler – Nordheim Tunneling – electrical thinning of oxide
- Defect Generation – Charge trapping due to high electric field

All of these mechanisms lead to increased leakage currents, however, when the electrical field is removed, they return to normal operation and have limited or no change in permanent conduction.

Stage 2

Soft Breakdown (SBD) (Noise Generation)

During this stage, leakage current is significantly increased but does not permanently damage the oxide. Unlike Hard breakdown (HBD), Soft breakdown (SBD) does not form a permanent leakage path.

Two fundamental conditions determine SBD:

- Sudden increase in leakage current though gate oxide
- An increase in gate signal noise.

Different phenomena can lead to the increased leakages of SBD.

Extreme trapped charge generation – When the high field is applied during programming, trapped charges begin to form conduction paths through the oxide. These paths can lead to a significant increase in leakage currents but not to Hard Breakdown.

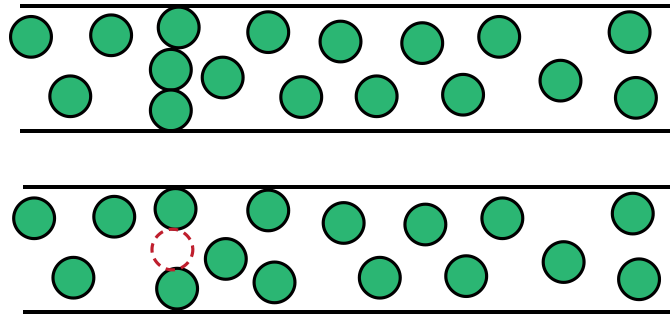


Figure 2

The above figure shows how either one or multiple paths can lead to the formation of a conduction path. Although these conduction paths change the current through the device, they do not physically change the oxide for permanent conduction. The conduction changes only after the electric field is removed or over time of operation and temperature changes.

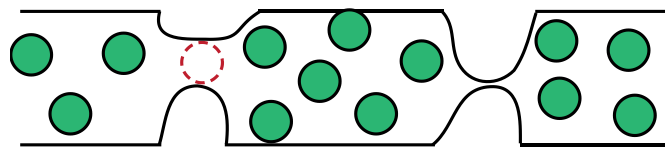


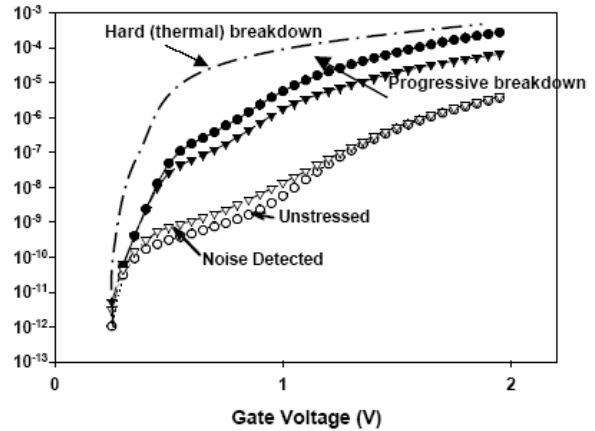
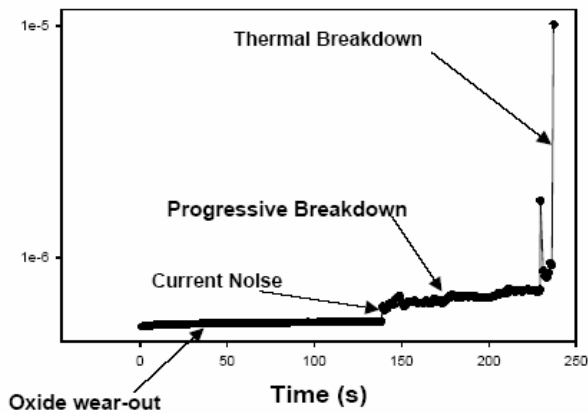
Figure 3

Oxide bumps can form at the top and bottom of the oxide also increasing leakage current but not forming a filament as pictured in Figure 2.

Stage 3

Hard Breakdown (HBD)

Hard Breakdown is an irreversible catastrophic breakdown of an oxide. Hard Breakdown is a severe case of soft breakdown where thermal runaway has resulted in a larger conduction path. After the current path, a permanent conduction path is established from the gate to channel.



The above charts demonstrate the initial conduction difference between Hard and Soft Breakdown; although small when compared to tunneling. Because of this difference, determining the point at which hard breakdown is achieved is very difficult.

Guaranteeing Hard Breakdown in Antifuse Memories

Antifuse OTP memory can be very reliable; however, certain antifuse technologies can still suffer yield problems if hard breakdown is not achieved. Since each programmed oxide is different from the next, every cell requires an individual programming time. Many antifuse vendors perform a statistical average for programming time and limit programming to the statistically averaged time. This method does not guarantee that each bit will be successfully programmed. Programming performed in this method will reduce the life of the part and requires redundancy to be added in order to maintain an acceptable yield percentage. In addition, a number of bits will never statistically reach hard breakdown. These bits are often referred to as “tail bits”. These tail bits can negatively affect yield and reliability.

In order to guarantee that hard breakdown is achieved, programming cannot be time based, but instead should be based on hard breakdown detection. Novocell’s patented SmartBit™ has the ability to detect hard breakdown on a bit by bit basis. This detection technology guarantees that hard breakdown is achieved. With the implementation of the SmartBit cell, Novocell offers 100% reliability with industry-leading data retention over 30 years.

Conclusion

In order to maximize reliability, sensing hard breakdown is crucial. Soft Breakdown closely resembles Hard Breakdown, but a static timed programming cannot guarantee that every bit has been programmed reliably. Hard Breakdown sensing eliminates the need for added redundancy to compensate for trapped charge dissipation over extended burn-in or device operation, a common problem when Hard Breakdown is not achieved in all bit cells.

For more information regarding Novocell's Novoblox™ OTP technology or Novocell's 2nTP multi-time write technology, please visit us at www.novocellsemi.com or send us an email at info@novocellsemi.com

Author Bio: Walter Novosel is the Engineering Director at Novocell Semiconductor. He has been in the industry 10 years focusing on NVM and Antifuse memories. He has helped guide Novocell to be the leader in reliability and performance in the antifuse OTP market.