

NovoBlox[®]



OTP Memory IP

Product Description

Novocell's NovoBlox[®] one-time programmable (OTP) memory IP is a non-volatile memory block which can be embedded in standard Logic CMOS without any additional process steps or post processing. It has the ability to be programmed at the package, circuit, or wafer level. NovoBlox is available in ROM and Serial architectures, and can be configured from 32bits up to 8Kbits.

New NovoBlox enhancements include smaller silicon areas, lower power operation, 10nsec or less read access times, increased margins at corners, and higher ambient temperature operation. Designed for the highest reliability, NovoBlox retains data for 10+ years.

Programming requires no additional or special hardware, and NovoBlox generates and confines the breakdown voltage entirely within the memory core. Unprogrammed cells are not subjected to voltage outside the native process parameters, and have the same reliability as the underlying CMOS technology. High voltage during programming is applied until the current signature of hard breakdown is detected, guaranteeing 100% programmability and data retention. NovoBlox is silicon proven at leading fabs including Jazz Semiconductor, Tower, TSMC, UMC, Silterra, and Chartered.

Applications

- Chip Configuration
- Analog Trimming and Calibration
- ID/Serial Numbers
- Encryption Keys
- Memory Redundancy
- Firmware Patches
- Code Patching
- Memory Repair

Features

- Highly reliable antifuse technology
- Standard logic CMOS without additional process steps
- Breakdown voltage contained entirely within memory core
- Wafer, in-package, or in-circuit programming
- >10 years data retention
- Routing over macros allowed
- Low programming current < 15 mA

Permanent Memory that Enables your Innovation...

Novocell Semiconductor, Inc – 3050 Prosperity Place – Hermitage, PA 16148

Phone: 724-983-0600 Fax: 724-983-1011

Web: www.novocellsemi.com email: info@novocellsemi.com

Products Specifications

Custom aspect ratios can be provided. Please visit www.novocellsemi.com for more information.

Serial Architecture

Ideal for fuse replacement

Technology	Bits	V _{dd} / V _{pgm} (Volts)	Part Number
180nm	32	1.8 / 3.3	NB32_180
	64	1.8 / 3.3	NB64_180
	128	1.8 / 3.3	NB128_180
	256	1.8 / 3.3	NB256_180
130nm	32	1.2 / 3.3	NB32_130
	64	1.2 / 3.3	NB64_130
	128	1.2 / 3.3	NB128_130
	256	1.2 / 3.3	NB256_130
90nm	32	1.0 / 2.5	NB32_090
	64	1.0 / 2.5	NB64_090
	128	1.0 / 2.5	NB128_090
	256	1.0 / 2.5	NB256_090

ROM Architecture

A natural fit for a processor-based system.

Technology	Total Bits	Word Size	V _{dd} / V _{pgm} (Volts)	Part Number
180nm	256	16	1.8 / 3.3	NB16x16_180
	1024	16	1.8 / 3.3	NB64x16_180
	1024	8	1.8 / 3.3	NB128x8_180
	2048	8	1.8 / 3.3	NB256x8_180
	4096	8	1.8 / 3.3	NB512x8_180
	4096	16	1.8 / 3.3	NB256x16_180
	4096	32	1.8 / 3.3	NB128x32_180
130nm	256	16	1.2 / 3.3	NB16x16_130
	1024	8	1.2 / 3.3	NB128x8_130
90nm	256	16	1.0 / 2.5	NB16x16_090
	1024	8	1.0 / 2.5	NB128x8_090

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