

# NovoBlox<sup>®</sup>



OTP Memory IP

## Product Description

Novocell's NovoBlox<sup>®</sup> one-time programmable (OTP) memory IP is a non-volatile memory block which can be embedded in standard Logic CMOS without any additional process steps or post processing. It has the ability to be programmed at the package, circuit, or wafer level. NovoBlox is available in ROM and Serial architectures, and can be configured from 32bits to 8Kbits.

New NovoBlox enhancements include smaller silicon areas, lower power operation, 10nsec or less read access times, increased margins at corners, and higher ambient temperature operation. Recognized for the highest reliability, NovoBlox retains data for 30+ years.

Programming does not require an external charge pump. NovoBlox generates and confines the breakdown voltage entirely within the memory core. Unprogrammed cells are not subjected to voltage outside the native process parameters, and have the same reliability as the underlying CMOS technology. High voltage during programming is applied until the current signature of hard breakdown is detected, guaranteeing 100% programmability and data retention. NovoBlox is silicon proven at leading fabs including Chartered, IBM, TowerJazz, TSMC, SilTerra, and UMC.

## Applications

- Chip Configuration
- Analog Trimming and Calibration
- ID/Serial Numbers
- Encryption Keys
- Memory Redundancy
- Firmware Patches
- Code Patching
- Memory Repair

## Features

- 100% Reliability- No Tail Bit Failures
- 30+ years Data Retention
- No External Charge Pump Required
- DONE Programming Signal
- Industry Leading Performance
- Access times <8nsec
- Foundry and Process Independent
- Low Programming Current < 15 mA

*Enabling your Innovation...*

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## Product Specifications

Custom aspect ratios can be provided. Please visit [www.novocellsemi.com](http://www.novocellsemi.com) for more information.

## Serial Architecture

Ideal for fuse replacement

Technology	Bits	V <sub>dd</sub> / V <sub>pgm</sub> (Volts)
180nm	32	1.8 / 3.3
	64	1.8 / 3.3
	128	1.8 / 3.3
	256	1.8 / 3.3
130nm	32	1.2 / 3.3
	64	1.2 / 3.3
	128	1.2 / 3.3
	256	1.2 / 3.3
90nm	32	1.0 / 2.5
	64	1.0 / 2.5
	128	1.0 / 2.5
	256	1.0 / 2.5

## ROM Architecture

A natural fit for a processor-based system.

Technology	Total Bits	Word Size	V <sub>dd</sub> / V <sub>pgm</sub> (Volts)
180nm	256	16	1.8 / 3.3
	1024	16	1.8 / 3.3
	1024	8	1.8 / 3.3
	2048	8	1.8 / 3.3
	4096	8	1.8 / 3.3
	4096	16	1.8 / 3.3
	4096	32	1.8 / 3.3
130nm	256	16	1.2 / 3.3
	1024	8	1.2 / 3.3
90nm	256	16	1.0 / 2.5
	1024	8	1.0 / 2.5

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